

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL J. ALLEN and STEPHEN F. SULLIVAN

Appeal No. 1997-0278
Application No. 08/367,917¹

ON BRIEF

Before HAIRSTON, FLEMING, and DIXON, **Administrative Patent Judges**.
DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1-6, 9-12, 14, 16 and 17, which are all of the claims pending in this application.

We REVERSE.

¹ Application for patent filed January 3, 1995.

BACKGROUND

The appellant's invention relates to a novel device structure for high voltage tolerant transistors on a 3.3 volt process. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced below.

1. A low voltage integrated circuit comprising:
 - a P- doped substrate material;
 - a first transistor device having
 - an N- doped well region in the P- substrate material,
 - an N+ doped drain terminal region in the N- well region,
 - an N+ doped source terminal region in the P- substrate material,
 - and
 - a gate separated from the source and drain terminal regions by a layer of silicon dioxide;
 - a second transistor device having
 - an N+ doped drain terminal region in the P- substrate material, the N+ doped drain terminal region joining the N+ doped source terminal region of the first transistor device,
 - an N+ doped source terminal region in the P- substrate material,

and

a gate separated from the source and drain terminal regions by a layer of silicon dioxide;

first conductive means connecting the drain terminal region of the first transistor device to a high voltage node to be discharged, wherein the high voltage node has a voltage of approximately 7-12 volts;

second conductive means connecting the gate of the first transistor device to a biasing potential equal to an operating voltage of approximately 3 volts used in a low voltage integrated circuit,

third conductive means connecting the source terminal region of the second transistor device to a ground potential; and

means for providing a positive input potential to the gate of the second transistor device to enable the first and second transistor devices and discharge the high voltage node without causing breakdown of the silicon dioxide layers or any junction of the first and the second transistor devices.

The prior art references of record relied upon by the Examiner in rejecting the appealed claims are:

Lee et al. (Lee)	4,922,311	May 01, 1990
Sato et al. (Sato)	5,016,077	May 14, 1991
Yamamoto	5,239,197	Aug 24, 1993

Claims 3, 5, 6 and 10 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sato. Claims 1-6, 9, 10, 16 and 17 stand rejected under 35 U.S.C.

§ 103 as being unpatentable over Sato in view of Lee. Claims 11 and 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sato in view of Yamamoto. Claims

11, 12 and 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sato in view of Lee and Yamamoto.

Rather than reiterate the conflicting viewpoints advanced by the Examiner and the appellants regarding the above-noted rejections, we make reference to the Examiner's answer (Paper No. 14, mailed July 19, 1996) for the Examiner's complete reasoning in support of the rejections, and to the appellants' brief (Paper No. 13, filed May 17, 1996) for the appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by the appellants and the Examiner. As a consequence of our review, we make the determinations which follow.

Appellants argue that Sato does not teach the discharge of a high voltage, approximately 7-12 volts, at a node across a low voltage transistor to ground as set forth in independent claims 1, 3, 6, 11 and 16. (See brief at page 6.) Appellants also argue that the 5 volts taught by Sato is not approximately 3 or 7 volts with reference to a low voltage circuit or switch. (See brief at page 6.) We agree with appellants. The language in each of independent claims 1, 3, 6, 11 and 16 includes a limitation in varied scope pertaining to the biasing of the transistors to allow the two transistors to

discharge 7-12 volts without damaging the low voltage circuit. (See brief at page 6.) Sato does not teach or suggest this claimed transistor configuration and biasing thereof as set forth in claims 1, 3, 6, 11 and 16 and we will not sustain the rejection of these claims.

The Examiner further includes Lee to teach the common source and drain of the two transistors with the motivation “to reduce transistor area.” (See answer at page 5.)

Appellants argue that Lee teaches away from the present invention. (See brief at page 7.)

We disagree with appellants with respect to teaching away, but agree that Lee does not

teach or suggest those features or motivations lacking in Sato. Appellants argue that

“Appellants’ invention uses an extended N- doped well to create a gradual junction,

between the drain and substrate region. Appellants’ gradual junction combined with

Appellants’ biasing means allow Appellants’ device to withstand relatively large voltage

differences.” (See brief at page 8.) We agree that Lee is not

concerned with the formation of a gradual junction or biasing two transistors to discharge a

high voltage to ground.² Therefore, Lee does not supply the deficiencies of Sato.

Therefore, we will not sustain the rejection of claims 1-6, 9-10 and 16-17.

² We note that Sato suggests to the skilled artisan to use a gradual junction with low impurity concentration to “absorb part of the voltage applied between the source and drain.” (See Sato at col. 2.)

The Examiner adds Yamamoto as a teaching of the well known use of incorporating low voltage integrated circuits into a (micro)computer and the inherent circuitry associated with the microcomputer. (See answer at page 5.) Appellants argue that Yamamoto teaches a one-chip microcomputer with an EEPROM, and that Yamamoto teaches "the use of an elaborate array of substrate patterns with various resistances that are devised to pass the higher voltages required by the EPROM to ground." (See brief at pages 8-9.) Appellants argue that "it would not have been obvious to use the integrated circuit of Sato to perform such a function, i.e. pass the higher voltages required by the EPROM to ground. Additionally, as stated above in the discussion of Sato, Appellants further submit that it is not obvious whether or not the integrated circuit of Sato could even withstand such a voltage." (*Id.* at 9.) We agree with appellants and further agree that Yamamoto does not teach or suggest those features or motivations lacking in Sato. Therefore, we will not sustain the rejection of claims 11 and 14.

Appellants argue that the combination of Sato, Lee and Yamamoto does not teach or suggest the low voltage switch or computer as set forth in claims 11, 12 and 14. We agree with appellants. As discussed above Yamamoto or Lee does not teach

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or suggest those features or motivations lacking in Sato. Furthermore, we find that the combination of Lee and Yamamoto does not teach or suggest those features or motivations lacking in Sato. Therefore, we will not sustain the rejection of claims 11-12 and 14.

To summarize, the decision of the Examiner to reject claims 1-6, 9-12, 14, 16 and 17 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON
Administrative Patent Judge

MICHAEL R. FLEMING
Administrative Patent Judge

JOSEPH L. DIXON
Administrative Patent Judge

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